

Precision capacitors for complementary metal oxide semiconductor (CMOS) analog applications are generally metal-insulator-metal (MIM) capacitors or polysilicon-insulator-polysilicon (P-P) capacitors. P-P capacitors are becoming less popular, however, because of the problems connected with their use in conjunction with complementary metal oxide semiconductor (CMOS) technologies. More specifically, P-P capacitors are generally fabricated before CMOS structures, and the heat and oxidation cycles of the CMOS fabrication process degrade P-P capacitors. In addition, as analog circuits

become more sophisticated, the allowed variation in the capacitance decreases and is preferably maintained at approximately 50 ppm/V. Because P-P capacitors suffer from carrier depletion (which changes the capacitance) as surface voltage across the P-P capacitor changes, P-P capacitors do not maintain the linearity required in sophisticated analog circuits. Further, P-P capacitors often trap charge within the dielectric during their use.

As a result, MIM capacitors, which are usually formed after the CMOS fabrication process, are becoming more popular for analog circuits. However, MIM capacitors also present manufacturing challenges, especially when used with copper wiring, because copper generally cannot be used as an electrode with an SiO₂ dielectric layer. In particular, the present invention recognizes that the etching step(s) utilized to define the simplest MIM capacitor that does not use the underlying damascene metallurgy as an electrode etches the top and bottom plates and the dielectric in one step, and in doing so, creates contamination on the edge of the dielectric that contacts both plates. This contamination is not easy to remove and causes undesirable leakage between the top and bottom plates.

SUMMARY OF THE INVENTION

In view of the foregoing, the present invention provides an improved capacitor structure and method of fabricating a capacitor structure that prevents a contamination layer formed during etching from connecting the top and bottom plates and thereby causing leakage.

A capacitor structure in accordance with the present invention includes a bottom plate, a top plate, and a dielectric layer between the bottom and top plates. In addition, at least one insulating sidewall spacer that protects the dielectric layer during processing is formed along the perimeter of the top plate and overlaying a portion of the dielectric layer. In a preferred embodiment, the sidewall spacer, which may be an oxide insulator, is formed following an etch of the top plate to expose the dielectric layer.

All objects, features, and advantages of the present invention will become apparent in the following detailed written description.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 depicts a side view of a substrate having a metal damascene layer formed therein;

Figure 2 illustrates a side view of a metal-insulator-metal (MIM) capacitor structure formed over a metal damascene layer in accordance with the present invention, after the layers needed to form the capacitor have been deposited;

Figure 3 depicts a side view of a MIM capacitor structure following a top plate etch;

Figure 4 illustrates a side view of a MIM capacitor structure following formation of an insulating layer;

Figure 5 depicts a side view of a MIM capacitor structure following formation of sidewall spacers that protect the dielectric layer;

Figure 6 depicts a side view of a MIM capacitor structure following etching of the dielectric layer and

bottom plate;

Figure 7 illustrates a side view of a completed
-MIM capacitor in accordance with the present invention;
and

Figure 8 depicts a high level flowchart of a
preferred process for fabricating a MIM capacitor in
accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to the figures and in particular with reference to **Figure 1**, there is illustrated a side view of a semiconductor substrate 10 (such as tantalum nitride (TaN), for example) in which openings are formed using conventional masking and etching processes. Metal damascene conductors 20, 21 are then deposited in the openings, and the resulting structure is planarized using, for example, chemical mechanical polishing (CMP). In the preferred embodiment, metal damascene conductors 20, 21 are formed of copper, although other metals such as gold are also suitable. Subsequently, a silicon nitride (Si_3N_4) layer 30 is formed over metal damascene layers 20, 21 and semiconductor substrate 10. Silicon nitride layer 30 is subsequently masked and etched to form an opening 25 in silicon nitride layer 30 to define the location at which a metal-insulator-metal (MIM) capacitor will be formed. The MIM capacitor may be formed without silicon nitride layer 30 if an etch process for the capacitor's bottom plate can be found that does not damage metal damascene conductor 21 when the capacitor layers are defined, as discussed further below.

Referring now to **Figure 2**, there is depicted a side view of a MIM capacitor structure formed over metal damascene conductor 20 in accordance with the present invention. As shown in **Figure 2**, a first barrier layer 40 such as tantalum nitride (TaN) may be formed over the silicon nitride layer 30 and in opening 25 such that

first barrier layer 40 contacts metal damascene conductor 20. First barrier layer 40 retards diffusion of copper (or other metal) from metal damascene conductor 20 into the capacitor's bottom plate and dielectric layer. A bottom electrode 50, which is preferably a thin layer of aluminum (Al), tungsten (W) or other suitable metal, is then formed over first barrier layer 40. A second barrier layer 60, such as titanium nitride (TiN), may then be formed over the bottom electrode 50. Second barrier layer 60 retards diffusion of the metal in bottom electrode 50 into dielectric layer 70. First barrier layer 40, bottom electrode 50, and second barrier layer 60 together form the bottom plate of the capacitor.

A dielectric layer 70, which is preferably made of silicon dioxide (SiO_2), may then be formed over second barrier layer 60, and a third barrier layer 80, which is preferably formed of titanium nitride (TiN), may then be formed over dielectric layer 70. Overlaying third barrier layer 80 is a top electrode 90 formed of aluminum or any other suitable metal. **Figure 2** further illustrates that a fourth barrier layer 100, formed of tantalum nitride (TaN) or other suitable barrier material, may be formed over top electrode 90. Third barrier layer 80, top electrode 90, and fourth barrier layer 100 together form the top plate of the capacitor. Over the top of the MIM capacitor structure, a silicon dioxide (SiO_2) or other insulator layer 110 is thereafter preferably formed to prevent charge leakage.

The foregoing layers can be formed using any

conventional process, such as chemical vapor deposition (CVD), sputtering, evaporation, etc. If the conductivity of barrier layers 100 and 40 is sufficient (i.e., the resistivity is not too high), then layers 30, 60 and 80 may be omitted from the MIM capacitor structure.

Following the formation of the MIM capacitor structure illustrated in **Figure 2**, portions of the various layers are removed in order to define a MIM capacitor of the desired size, as described in detail below with respect to **Figures 3-7**. Generally, in order to reduce process steps, conventional capacitors have been defined by a continuous etching process that etches through the top plate, dielectric layer and bottom plate, stopping on the underlying substrate. However, as noted above, this conventional etching process exposes the capacitor dielectric surface at the perimeter of the plates during etching, which leads to contamination forming a connection between the top and bottom plates of the capacitor. As a result, undesirable charge leakage occurs between the top and bottom plates of the capacitor. Accordingly, the present invention forms at least one protective sidewall spacer that encloses the top plate (e.g., layers 80, 90 and 100) in a protective insulator coating, while the capacitor dielectric (e.g., layer 70) and bottom plate (e.g., layers 40, 50 and 60) are etched.

Referring now to **Figure 3**, after the formation of the layers of the MIM capacitor structure discussed above, a photo mask 120 is applied over the MIM capacitor structure and patterned utilizing conventional techniques.

Photo mask **120** defines the geometry and location of the capacitor top plate. An etch of layers **110**, **100**, **90** and **80** is then performed, with the etch stopping at the interface between dielectric layer **70** and third barrier layer **80** (or top electrode **90**, if third barrier layer **80** is omitted). Photo mask **120** is thereafter stripped away.

Next, as depicted in **Figures 4 and 5**, to protect dielectric layer **70** during later etching, a conformal layer of an insulator **130** such as silicon dioxide (SiO_2) is formed (e.g., deposited) and then etched to form one or more sidewall spacers **132a** and **132b** surrounding the perimeter of the top plate (e.g., layers **80**, **90** and **100**) and insulator **110**. Thus, when dielectric layer **70** and the bottom plate (e.g., layers **40**, **50** and **60**), are subsequently etched, as illustrated in **Figure 6**, sidewall spacers **132** prevent contamination from the etching process connecting the top plate (e.g., layers **80**, **90** and **100**) to the bottom plate (e.g., layers **30**, **40** and **50**) and causing charge leakage.

Subsequently, as shown in **Figure 7**, a barrier layer **134**, preferably made of silicon nitride (Si_3N_4), may be applied over the top and sides of the MIM capacitor using conventional deposition techniques such as those mentioned above to thereby surround portions of the capacitor stack (and specifically dielectric layer **70**). An interlayer dielectric (ILD) **136** is then deposited over the entire MIM capacitor stack and may be subsequently planarized using processes well known in the art, such as CMP. Thereafter, the MIM capacitor is ready for via

connections **150** to both top plate of the metal-insulator-metal capacitor and metal damascene conductor **21** using processes well known in the art, such as lithographic masking, etching and conductive stud formation. Via connections **150** may be further connected to a next layer of metal damascene wiring **140**.

Referring now to **Figure 8**, there is illustrated a flowchart of a preferred method of forming a MIM capacitor in accordance with the present invention. The process begins at block **160** and thereafter proceeds to block **162**, which illustrates the formation of metal damascene conductors **20, 21** in semiconductor substrate **10**. Next, at block **164**, Si_3N_4 layer **30** is formed over substrate **10**, and an opening is etched in Si_3N_4 layer **30**. As noted above, if overetching of metal damascene conductors **20-21** is not a concern, then block **164** can optionally be omitted. A first barrier layer **40** is then added at block **166** that contacts metal damascene conductor **20**. At block **168**, the remainder of the MIM capacitor structure is formed by sequentially forming bottom electrode **50**, second barrier layer **60**, dielectric layer **70**, third barrier layer **80**, top electrode **90** and fourth barrier layer **100**. In addition, an overlying insulator layer **110** may optionally be formed in order to retard charge leakage.

Thereafter, as depicted at block **170**, a photo mask **120** is utilized to pattern capacitor top plate (e.g., layers **80, 90** and **100**) in an etch back of the capacitor stack stopping on dielectric layer **70**. Next, as shown at block **172**, one or more sidewall spacers **132** are formed

around the perimeter of the top plate and over dielectric layer 70 through the deposition and etching of silicon dioxide, for example. Sidewall spacers 132 protect dielectric layer 70 from overetching and contamination during the subsequent etch of dielectric layer 70 and the bottom plate (e.g., layers 40, 50 and 60), which is depicted at block 174. The etch of the bottom plate stops on silicon nitride layer 30, if present.

After the essential structure of the MIM capacitor has been defined by the foregoing etching steps, capacitor fabrication continues at block 176, which depicts forming silicon nitride layer 134 on the top and sides of the capacitor stack and depositing and planarizing interlayer dielectric 136. Finally, as illustrated at block 178, contacts 150 to the top plate and metal damascene conductor 21 are formed, and wiring 140 is deposited in a conventional manner. Thereafter, the process ends at block 180.

As has been described, the present invention provides an improved capacitor and method of capacitor fabrication that reduce charge leakage between the capacitor plates by protecting the capacitor dielectric with insulating sidewall spacers during etching.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. In

particular, those skilled in the art will appreciate that the formation of protective sidewall spacers in accordance with the present invention, although particularly suitable for use in MIM capacitor fabrication, may also be employed in the fabrication of types of capacitor structures.

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